ABSTRACT OF THE DISCLOSURE

An apparatus for killing an instruction after it has already been loaded into an instruction queue of a microprocessor is disclosed. The apparatus includes control logic that detects a condition in which the instruction must not be executed, such as a branch instruction misprediction; however, the control logic determines the condition too late to prevent the instruction from being loaded into the instruction queue. The control logic generates a kill signal indicating the instruction must not be executed. A kill queue receives the kill signal and stores its value. The kill queue maintains its entries in parallel with the instruction queue entries so that when the instruction queue subsequently outputs the instruction, the kill queue also outputs the value of the kill signal associated with the instruction. If the kill signal value output from the kill queue is true, then the microprocessor invalidates the instruction and does not execute it.